Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, Nov/Dec - 2016
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Convert $(101.11011)_2$ into Decimal, Octal, Hexadecimal (4M)
   b) What are the basic differences between a branch instruction, a call subroutine instruction and program interrupt (4M)
   c) For a RISC machine, the effective value of S is 1.25 and the average value of N is 200. If the clock rate is 500MHz, calculate the total program execution time (4M)
   d) Explain the hardware implementation for Booth algorithm (4M)
   e) Explain the principle of virtual memory (3M)
   f) What is the need of I/O interface module (3M)

PART –B

2. a) With the help of a block diagram, explain the process of addition/subtraction using two's complement number (8M)
   b) Describe about the Fixed point representation of numbers with an example (8M)

3. a) Draw the block diagram of arithmetic logic shift unit and explain its operations (8M)
   b) Explain the instruction cycle with an example (8M)

4. a) What do you mean by Addressing modes? Explain the following addressing modes: (10M)
      i) Index Addressing mode ii) Immediate Addressing mode
      iii) Relative Addressing mode iv) Direct Addressing mode
   b) Compare the hard wired control unit and micro programmed control unit (6M)

5. a) Show the step by step multiplication process using Booth algorithm when the following binary numbers are multiplied (+15) * (-13). Assume 5-bit registers that hold signed numbers and draw the flow chart for the corresponding example (10M)
   b) Draw the flow chart for division algorithm (6M)

6. a) Compare and contrast between Asynchronous DRAM and Synchronous DRAM. (8M)
   b) What is cache memory? Explain the different mapping functions (8M)

7. a) What do you mean by inter process arbitration? Explain how it is implemented in multiprocessor architecture (8M)
   b) Explain the method of DMA transfer. How does a DMA controller improve the performance of a computer (8M)

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